REMARKS

This application has been carefully reviewed in light of the office action mailed October 15, 2003. Claims 1-11 and 26-33 are pending in this application. Support for amendment of independent claims 1 and 26 can be found in paragraph 27. Applicants believe that this amendment places the claims in better form for allowance or consideration on appeal, and respectfully request its admission.

Rejections under 35 USC §103

Claims 1-2, 5-6 and 8-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 5,640,041 issued to Lur et al. (hereinafter Lur).

Claim 1 recites among other things, a semiconductor device (e.g., 2) comprising a first dielectric material (e.g., 60) deposited in a first recessed region and formed with a second recessed region (e.g., 76), and a second dielectric material (e.g., 100) thermally grown over the first dielectric material to seal the second recessed region, wherein a wall (e.g., 92) of the second recessed region is substantially absent second dielectric material.

The Lur '041 reference discloses in Fig. 6 trench 19 formed in deposited silicon dioxide 24, a layer 25 of chemical vapor deposition (CVD) silicon dioxide deposited within and over the Lur trenches to form voids 30.

The examiner states on page 2 of the office action that thermally grown and CVD dielectric layers are functionally equivalent in terms of sealant atop trenches. While it is true that both materials function as a sealant, there are significant inherent structural differences between them. In the case where the dielectric material is silicon dioxide, a thermally grown layer is more dense and structurally stronger than a deposited layer. Moreover, the reaction that forms the layer is highly conformal and localized when the material is thermally grown, whereas CVD material is deposited uniformly over the entire surface of the wafer. Therefore, in the Lur device, because its sealant is a deposited silicon dioxide, a substantial portion of the sealant material is deposited within the trench and on the trench wall (Figures 7, 10 and 13) reducing the size of the voids. In contrast, the claimed sealant material is thermally grown, and therefore localized to the region above the trenches, which means material does not substantially accumulate within the trench, as explained in paragraph **[0027]** on page 8, lines 13-17. Thus the claimed trench wall is substantially absent sealant material. Consequently the claimed semiconductor device has a lower effective dielectric constant and capacitance.

Thus, the applicants recitation of thermally grown dielectric material is believed to constitute a key structural element not found in the Lur reference. Furthermore, the applicants recitation of a wall of the second recessed region (e.g., trench) substantially absent second dielectric material is believed to constitute an

additional key structural element not found in the Lur reference.

Therefore, claim 1 is not believed anticipated by the Lur reference and should be in condition for allowance or for consideration on appeal per Title 37 CFR §1.116. Original claims 2-11 depend from original claim 1, and are therefore allowable for at least the same reasons.

Claim 26

Claim 26 is rejected under 35 U.S.C. §103(a) as being unpatentable over Lur et al. in view of Wolf ("Silicon Processing for the VLSI Era: Volume 2- Process Integration," Latice Pres, Sunset Beach, CA, (1990),pp.196-197 (hereinafter Wolf).

Claim 26 recites among other things, a semiconductor device comprising a first dielectric material (e.g., 60) deposited in a first recessed region (e.g., 20) and formed with a second recessed region (e.g., 76), a first semiconductor layer (e.g., 75) deposited over and between the second recessed region, and a second dielectric material (e.g., 100) thermally grown on the first semiconductor layer to seal the second recessed region, wherein a wall of the second recessed region is substantially absent second dielectric material.

As discussed above, the Lur reference discloses trenches formed in deposited silicon dioxide and sealed with deposited silicon dioxide within and on the trench to form voids.

The Wolf reference discloses void formation by the shadowing effect, wherein the Wolf deposited CVD material

forms the walls of the void and the seal (refer to Fig. 4-8).

However, neither the Lur reference nor the Wolf reference, show or teach a dielectric layer thermally grown on a semiconductor layer to seal a recessed region wherein a wall of the recessed region is substantially absent sealing material as claimed. As stated above, thermally grown dielectric material is believed to be patentably distinct from deposited material, both in its density and in the residue deposited on other regions of the device.

For the foregoing reasons, new claim 26 is believed to be patentably distinct from the references cited, and therefore claim 26 should be in condition for allowance or for consideration on appeal per Title 37 CFR §1.116. Since new claims 27-33 depend from claim 26, they should be allowable for at least the same reasons.

Applicants respectfully believe the rejection to have been overcome.

Conclusion

Applicants have made an earnest attempt to place this case in condition for allowance. In light of the above remarks, applicants respectfully request reconsideration and allowance of claims 1-11 and 26-33.

Applicants have reviewed the other prior art made of record and believe that such art does not affect the patentability of the claimed invention. Applicants respectfully request entry of this amendment and early and favorable acceptance of this application.

If there are matters that can be discussed by telephone to further the prosecution of this application, applicants invite the examiner to call the undersigned attorney at the examiner's convenience.

Respectfully submitted,

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Date: 1/15/04